

What Is Claimed Is:

1. A processor comprising:

a plurality of program counters;

one or a plurality of instruction execution parts; and

5 means for selectively supplying for a plurality of threads instruction flows to said one or a plurality of instruction parts, each of said threads corresponding each of said program counters,

10 wherein said threads can be executed either simultaneously or in time multiplex,

wherein said processor has changeable execution priorities among said threads in time multiplex and generates the same result as serial execution according to said priorities would generate.

15 2. The processor, according to Claim 1, whereby it is made possible to reduce hardware volume of said processor and data deliveries between said threads through a shared resource by causing said threads to share part or the whole of processor resources except said program counters.

20 3. The processor, according to Claim 1, wherein the processor hardware is enabled to achieve synchronization among said threads without requiring any intervening instruction by using the number of repeats as a first criterion of priority and priorities among said threads as a second criterion of
25 priority.

4. The processor, according to Claim 1, further comprising a buffer for temporarily holding the execution results of threads other than that having top priority,

thereby making possible conflict-free execution of such other threads by storing them in their primary storing location after the completion or synchronization report of processing with higher priority.

5. The processor, according to Claim 1, wherein the use of undefined data can be eliminated and threads other than that having top priority can be executed without a conflict by confining data dependency among said threads so that data flow in only one direction and executing a data using thread only when it is the top priority thread.

6. The processor, according to Claim 1, wherein a storing location for data to be used in inter-thread data communication is confined.

7. The processor, according to Claim 6, wherein a plurality of locations are defined for data storage, independent of each and differentiated by the combination of threads and the direction of communication.

8. The processor, according to Claim 7, wherein an execution priority is defined for each of said data storing locations.

9. The processor, according to Claim 6, wherein said data storing location is part of a register or memory.

10. The processor, according to Claim 1, further having a thread priority raising instruction for threads lower in priority to facilitate changing priority among said threads.

11. The processor, according to Claim 1, further having
5 a data definition synchronizing instruction for other threads to make possible the use of data by other threads after synchronization.

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